In other words, as many memory cells MC are connected to each bus line as there are groups within the memory cell array. Only the selected group can bring the signals corresponding to the stored data onto the bus line.

Consequently, it is possible to dispense with the customarily provided multiplexer, which had to be used, during each read cycle, to select from the read data corresponding to a complete row of the memory cell array those data actually intended to be outputted.

Although, in the case of the described configuration and the described addressing method, it is necessary to provide a decoder which, using the address to be read out from the memory, determines the group to be selected. That is to say, it determines the group whose source line SL, in contrast to all the other source lines SL, is to have applied to it a potential suitable for reading. Such decoders are extremely simple and small in their structure so that the outlay to be accepted as a result is completely negligible.

The above description, in particular that of FIG. **2**, refers primarily to the fact that all of the memory cell groups of a memory cell array are the same size. However, this is not a necessary condition. Rather the memory cell groups can differ from one another and be as large as desired. The number of memory cells MC of the largest memory cell group should then correspond, however, to the number of bus lines provided as described.

It is also possible notably and advantageously to employ the effect that when the bus line is simultaneously connected to a plurality of selected memory cells (from the same or different memory cell groups), it can simultaneously assume the function of an OR or EXCLUSIVE-OR element.

The structure of the read-only memory according to the invention and the inventive method for addressing the same were explained above with reference to a ROM. However, the same effects and advantages of the measures described can also be achieved when providing the same in other types of read-only memories (PROM, EPROM, EEPROM, etc.).

I claim:

1. A read-only memory, comprising:

word lines, bit lines and source lines, each of said bit lines having a bit line potential;

a multiplicity of memory cells connected to said word lines, said bit lines and said source lines, said memory cells having data contents and the data contents being read out with appropriate addressing of said word lines, said bit lines and said source lines, said memory cells addressed by an individual word line;

said memory cells divided into a multiplicity of memory cell groups, each of said memory cell groups having a separate common source line, said memory cell groups forming a memory cell array;

common data output lines, each memory cell group connected to a respective one of said common data output lines; and

connecting devices connected between said bit lines of said memory cells of said memory cell groups and said common data output lines for outputting the data contents stored in said memory cells, each of said connecting devices for putting a potential that is on one of said bit lines onto one of said common data output lines at the beginning of a read cycle while said one bit line is discharging and for subsequently actively driving said one bit line.

2. The read-only memory according to claim **1**, wherein at least some of said memory cells each have at least one transistor.

3. The read-only memory according to claim **1**, wherein said memory cells are each connected to a word line, a bit line and a source line.

4. The read-only memory according to claim **1**, wherein said memory cells are disposed in rows and said memory cells disposed in the same row of said memory cell array are each connected to the same word line.

5. The read-only memory according to claim **1**, wherein said memory cells are disposed in columns and said memory cells disposed in the same column of said memory cell array are each connected to the same bit line.

6. The read-only memory according to claim **1**, wherein said memory cells are disposed in columns and said memory cells disposed in the same column of said memory cell array are each connected to the same source line.

7. The read-only memory according to claim **1**, wherein each of said memory cells are configured for storing a data bit.

8. The read-only memory according to claim **1**, wherein each of said memory cell groups are configured for storing a data word formed of data bits.

9. The read-only memory according to claim **8**, wherein said data word is a data byte.

10. The read-only memory according to claim **1**, wherein said memory cells of a memory cell group are distributed over a row of said memory cell array.

11. The read-only memory according to claim **10**, wherein said memory cell groups formed in said row of said memory cell array are the same size.

12. The read-only memory according to claim **10**, wherein said memory cell groups formed in said row of said memory cell array are of different sizes.

13. The read-only memory according to claim **1**, wherein each of said data output lines is connected to separate connecting devices, each of said separate connecting devices are connected to one bit line per said memory cell groups.

14. The read-only memory according to claim **13**, wherein each of said memory cells is connected to precisely one of said data output lines.

15. The read-only memory according to claim **13**, wherein said data output lines are provided in a number which corresponds to a number of said memory cells in a largest memory cell group.

16. The read-only memory according to claim **13**, wherein said connecting devices are configured to allow only selected memory cells of said memory cells to output the data contents of said memory cells onto said data output lines.

17. The read-only memory according to claim **16**, wherein said connecting devices are each configured to actively switch a signal to a corresponding data output line when a respectively assigned bit line changes its potential in a predetermined direction.

18. A connection configuration, comprising:

a bus line and a bit line;

switches connected to a precharge line, said switches for switching said bus line to a first potential and said bit line to a second potential;

holding elements for holding potentials on said bit line and on said bus line, when said bit line and said bus line have been precharged; and

a further switch connected to said bit line for switching said bit line to a source line at said first potential and for switching said bus line to said second potential, when said bit line has been connected to the source line at said first potential.

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